



DFW
PATENTS
MIC-42

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicant : Seong-Hoon Lee
Application No. : 10/734,506 Confirmation No.: 1009
Filed : December 12, 2003
For : GENERATING MULTI-PHASE CLOCK SIGNALS
USING HIERARCHICAL DELAYS
Group Art Unit : 2816

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

TRANSMITTAL LETTER FOR
INFORMATION DISCLOSURE STATEMENT

Sir:

Transmitted herewith is an Information Disclosure Statement in the above-identified patent application. This Statement is submitted:

[] within three months of the application filing date;

[X] more than three months from the application filing date but before the mailing date of the first Office Action on the merits.

In accordance with 37 C.F.R. § 1.97(b)(3), submission of this Statement requires no fee. However, if for any reason a fee is due, the Director is hereby authorized to charge payment of any fees required in connection with this Information Disclosure Statement to Deposit Account No. 06-1075. A duplicate copy of this letter is transmitted herewith.

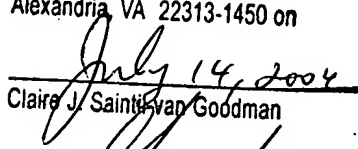
Respectfully submitted,

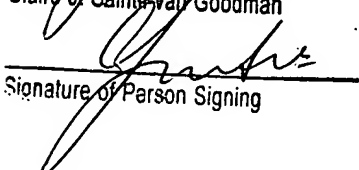

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Alexandria, VA 22313-1450 on


July 14, 2004
Claire J. Saint-Yvan Goodman


Signature of Person Signing



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INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicant hereby makes the following documents of record in
the above-identified patent applications:

U.S. Patent Documents

<u>Patent No.</u>	<u>Applicant (s)</u>	<u>Issued</u>
5,463,337	Leonowich	10/31/95
6,194,947	Lee et al.	02/27/01
6,295,328	Kim et al.	09/25/01
6,313,688	Lee et al.	11/06/01
6,326,826	Lee et al.	12/04/01
6,366,148	Kim	04/02/02

U.S. Patent Documents

<u>Patent No.</u>	<u>Applicant(s)</u>	<u>Issued</u>
6,512,408	Lee et al.	01/28/03
6,573,771	Lee et al.	06/03/03
6,642,760	Alon et al.	11/04/03
6,661,863	Toosky	12/09/03

U.S. Patent Application Publication

<u>Application No.</u>	<u>Applicant</u>	<u>Filed</u>
2003/0219088 A1	Kwak	12/30/02

Other Documents

Jong-Tae Kwak et al., A Low Cost High Performance Register-Controlled Digital DLL for 1 Gbps x32 DDR SDRAM, The 8th Korean Conference on Semiconductors, February 2001.

Ramin Farjad-Rad et al., A Low-Power Multiplying DLL for Low-Jitter Multigigahertz Clock Generation in Highly Integrated Digital Chips, IEEE Journal of Solid-State Circuits, Vol. 37, No. 12, December 2002, p. 1804-1812.

Copies of the aforementioned documents, which are listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith. It is respectfully requested that these documents be: (1) fully considered by the Patent and Trademark Office during examination of this application; and (2) printed on any patent which may issue on this application.

Applicant also wishes to call the attention of the Examiner to Lee, U.S. Application Nos. 10/719,348, filed

November 21, 2003, 10/722,959, filed November 26, 2003,
and 10/734,339, filed December 11, 2003 (copies of each
enclosed). These patent applications have not been listed on
the accompanying Form PTO-1449 to prevent their respective
Application Nos. from being printed on the face of any patent
issuing from the present application. Applicant respectfully
requests that the Examiner initial "All references have been
considered" on the enclosed Form PTO-1449 to indicate that
these references were considered. See MPEP §§ 609 III.C(2)-
(3).

Applicant requests that a copy of Form PTO-1449, as
considered and initialed by the Examiner, be returned with
the next communication.

Respectfully submitted,

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450 on

July 14, 2004
Claire J. Saint-Van Goodman

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FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MIC-42APPLICATION NO.
10/734,506INFORMATION DISCLOSURE STATEMENT
BY APPLICANTAPPLICANT
Seong-Hoon LeeCONFIRMATION NO.
1009FILING DATE
December 12, 2003GROUP
2816

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,463,337	10/31/95	Leonowich	327	158	
	6,194,947	02/27/01	Lee et al.	327	359	
	6,295,328	09/25/01	Kim et al.	375	376	
	6,313,688	11/06/01	Lee et al.	327	359	
	6,326,826	12/04/01	Lee et al.	327	161	
	6,366,148	04/02/02	Kim	327	262	
	6,512,408	01/28/03	Lee et al.	327	359	
	6,573,771	06/03/03	Lee et al.	327	158	
	6,642,760	11/04/03	Alon et al.	327	158	
	6,661,863	12/09/03	Toosky	375	376	
	2003/0219088 A1	12/30/02	Kwak	375	376	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
	Jong-Tae Kwak et al., A Low Cost High Performance Register-Controlled Digital DLL for 1 Gbps x32 DDR SDRAM, The 8th Korean Conference on Semiconductors, February 2001.
	Ramin Farjad-Rad et al., A Low-Power Multiplying DLL for Low-Jitter Multigigahertz Clock Generation in Highly Integrated Digital Chips, IEEE Journal of Solid-State Circuits, Vol. 37, No. 12, December 2002, p. 1804-1812.

All references have been considered.

EXAMINER INITIAL

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.